

**Department of Physics**

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| Course Number | COE 328 |
| Course Title | Digital Circuits |
| Semester/Year | Fall 2021 |
| Instructor | Dr. Reza Sedaghat |
| TA Name | Sajjad Rostami Sani |

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| Lab/Tutorial Report No. | 3 |
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| Report Title | Lab 3 |

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| Section No. | 03 |
| Submission Date | 31-10-2021 |
| Due Date | 01-11-2021 |

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**Objective**

The objective of this lab was to build a simple adder and subtractor circuit with a 7-segment display that takes 2 binary numbers in binary form and outputs their sum in the hexadecimal numerical system for part 1. For part 2 the circuit was modified to have an encoder which will display the respective digit of my student number, for example adding 2+3 is equal 5 so the circuit would output the 5th digit of my student number.

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**Procedure**

Part 1:

VHDL code for adder and subtractor unit:Text

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The code was copied from the textbook from figure 5.28. The only changes that were made to the code were the if and else statements from lines 14 to 30 to show a negative sign on the g segment of a second 7-segment display if the sum of the 2 numbers is negative to indicate that.

VHDL code for the 7-segment display:

Table

Description automatically generated with low confidence

The code was copied from the textbook from figure 6.47 and was modified to have lines from 27 to 32 to display the sum of the 2 binary numbers in hexadecimal form showing A for number 10 lowercase b for 11 C for 12 lower case d for 13 E for 14 and F for 15.

It was also modified to have a second process to turn on the g segment of a second 7-segment display to indicate that a number is negative when the carry in is 1.

Compiling both codes and generating a block component of each code and connecting them as the following circuit gives a simple adder subtractor circuit.

Calendar

Description automatically generated

Table

Description automatically generatedCompiling the circuit then running it in a wave function file to test if it is running correctly.

Adding Y and X which are “1” and “2” in binary form results in a “3” displayed on the first 7-segment display (lights up the a b c d and g segments) and nothing on the second since it is a positive number but when Y-X is implemented (Carry in is 1) the sum is “-1” so the process results in a “1” on the first 7 segment display (lights up the b and c segments) and a “–” on the second display since it is a negative number (lights up the g segment).

Part 2:

VHDL code for the encoder/combinatorial block circuit:

A picture containing table

Description automatically generated

L0 L1 L2 and L3 are resultant logical functions from the k-maps of the following table which’s outputs is based on my student number’s digits in binary system.

Table

Description automatically generated

5

0

1

0

1

1

8

5

2



A truth table and a k-map is made for each output L(n) and then simplified to a logical function.

Table

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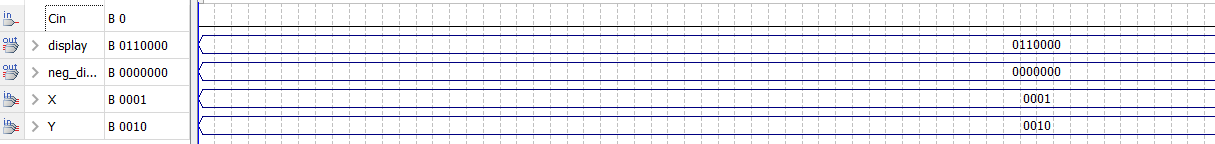
After compiling the code for this block circuit, the circuit is simple. It is very similar to the circuit from part 1 but with the encoder/combinatorial block circuit in between the ASU and the 2 7-segment displays.

Diagram

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The carry out and negative terminals are grounded because a position of a digit cannot be negative so these terminals should always carry a “0” signal since they must always be positive.

Running the wavefunction of this circuit:



Adding Y and X which are “1” and “2” in binary form is equal “3” which then goes through the encoder and displays the third number of my student number on the 7-segment display which is 1 lighting up the b and c segments and since it cannot be a negative number the second display shows nothing.

**References**

Brown, S. D., & Vranesic, Z. G. (2009). *Fundamentals of Digital Logic with VHDL Design*. New York, United States: McGraw-Hill Education.